Executive Post Graduate Certification in

AI-Enabled VLSI Design

(Low Power | AI-EDA Workflow)

By Indian Institute of Technology Kharagpur

- Executive Alumni Status of IIT Kharagpur
- 100 Hours of Cadence Tool Access
- 100% Live Online taught by IIT Kharagpur Faculty & Industry Experts
- 8 Months Program

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Architect the Silicon of Tomorrow: From Low-Power RTL to AI-Optimized GDSII

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About IIT Kharagpur

INDIA'S FIRST IIT | A Legacy of Excellence, Innovation, and Leadership

Established in 1951, IIT Kharagpur is **India's First Indian Institute of Technology** and a pioneer of technical education, research, and innovation in the country. Over the decades, it has set the benchmark for **Engineering Excellence, Academic Rigor, and Industry Relevance**, shaping generations of leaders, technologists, and innovators.

IIT Kharagpur is globally recognized for its **Cutting-edge Research, Strong Industry Collaboration, and Interdisciplinary Approach** to solving complex real-world problems. The institute consistently drives innovation across domains such as **Electronics, Semiconductor Technology, Computer Science, Manufacturing, and Applied Sciences**, contributing significantly to India's technological and economic growth.

With one of the **Largest and Most Diverse Academic Ecosystems in Asia**, IIT Kharagpur fosters a culture of **Critical Thinking, Collaboration, and Hands-on Learning**. Its programs combine strong theoretical foundations with practical application, ensuring graduates are equipped to lead in academia, industry, and entrepreneurship.

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Message from the Director

Prof. Suman Chakraborty
Director, IIT Kharagpur

*The **semiconductor industry** today is no longer looking for engineers who can simply operate tools. It demands professionals **who can Architect Systems, Understand Power as a Physical Constraint, Handle Performance at Scale**, and recognise the Growing Role of AI and Cloud Infrastructure in Modern Silicon Design.At IIT Kharagpur, we have designed this program to address that shift directly. The curriculum moves beyond isolated **RTL Coding** and simulation to focus on building engineers who can*
Design Systems that Withstand Real-world Silicon Constraints.

*This program is anchored in **Xilinx/Cadence's industry-standard EDA platforms,** ensuring learners work on the same **Synthesis, Timing, Physical Design, Power Analysis, and Signoff Flows** used in advanced semiconductor companies. Backed by IIT Kharagpur's long-standing strengths in semiconductor research and engineering education, the curriculum integrates **foundational design concepts with AI-driven fine-tuning** to reflect how chips are built today. This program represents our commitment to preparing engineers not just for their first role, but for long-term impact in the semiconductor ecosystem.*

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The 2026 Mandate

Why AI-EDA and Low Power?

The global semiconductor market is projected to be a **$1 Trillion industry by 2030**. However, 80% of current VLSI graduates lack **'Production-Ready with Agentic AI Orchestration'** literacy.

- **The Low-Power Requirement:** With edge AI and mobile growth, **Low-Power Design (UPF)** is no longer an elective; it's a requirement for survival.
- **The Productivity Requirement:** Industry leaders like Synopsys and Cadence are integrating AI. Learning **AI-Integrated EDA** is the only way to meet the aggressive Time-to-Market (TTM) demands of the future.
- **The Scale Crisis:** Physical hardware limits are gone. Prototyping has moved on, where verification happens at hyperscale.

FROM SILICON DESIGN TO SYSTEM INTELLIGENCE

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Beware the "Simulation Mirage"

The RTL design passes every testbench in a local simulator. But when synthesized for Silicon, the chip fails timing closure. The power leakage exceeds limits. The physical board arrives weeks late, stalling your verification.

The Reality

Local tools and "Basics-only" courses don't prepare you for the production floor. This program solves the "Reality Gap" by integrating:

- **Signoff-Grade Tools:** Using the Cadence-integrated flow for genuine PPA literacy.
- **AI-Guided Tuning:** Automating the bottleneck-heavy closure loops that manually take weeks.

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Program Snapshot

Duration

32 Weeks | 8 months

Format

100% Live Faculty-Led Online Sessions (5 Hrs/Week)

Core Learning Structure

Strong VLSI Foundations, AI in Chip Design, Industry Tool Mastery, Design-to-Deployment Thinking

Hands-On Experience using Vivado/Cadence design suite

Applied labs, design simulations, & real-world problem-solving scenarios aligned with semiconductor industry needs.

Capstone Project

Build a production-oriented VLSI solution that demonstrates real-world semiconductor design capability.

Credential

Earn **Executive Alumni Status*** from IIT Kharagpur.

*terms & conditions apply

The Transformation

(Before vs. After)

FEATURE	TRADITIONAL VLSI COURSES	IITKGP: HIGH-FIDELITY FUSION FLOW
Verification	Local simulation only	Hyperscale Simulations
Design Depth	Standard RTL Patterns	Power-Aware Architecture (UPF/ Clock Gating)
Tool Focus	Single-tool	Vivado/Cadence Signoff-Grade Flow
AI Integration	None	AI-Assisted DSE
Portfolio	Theoretical Projects	"Evidence-Packs": Verified Logs & Silicon Reports

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The 4 USPs

High-Fidelity Fusion Flow

We use the same tools as the world's top Foundries. You get the exposure of industry standard tools such as **Vivado/Cadence Tool chain** integrated with industry-standard practices.

The "Power-First" Lever

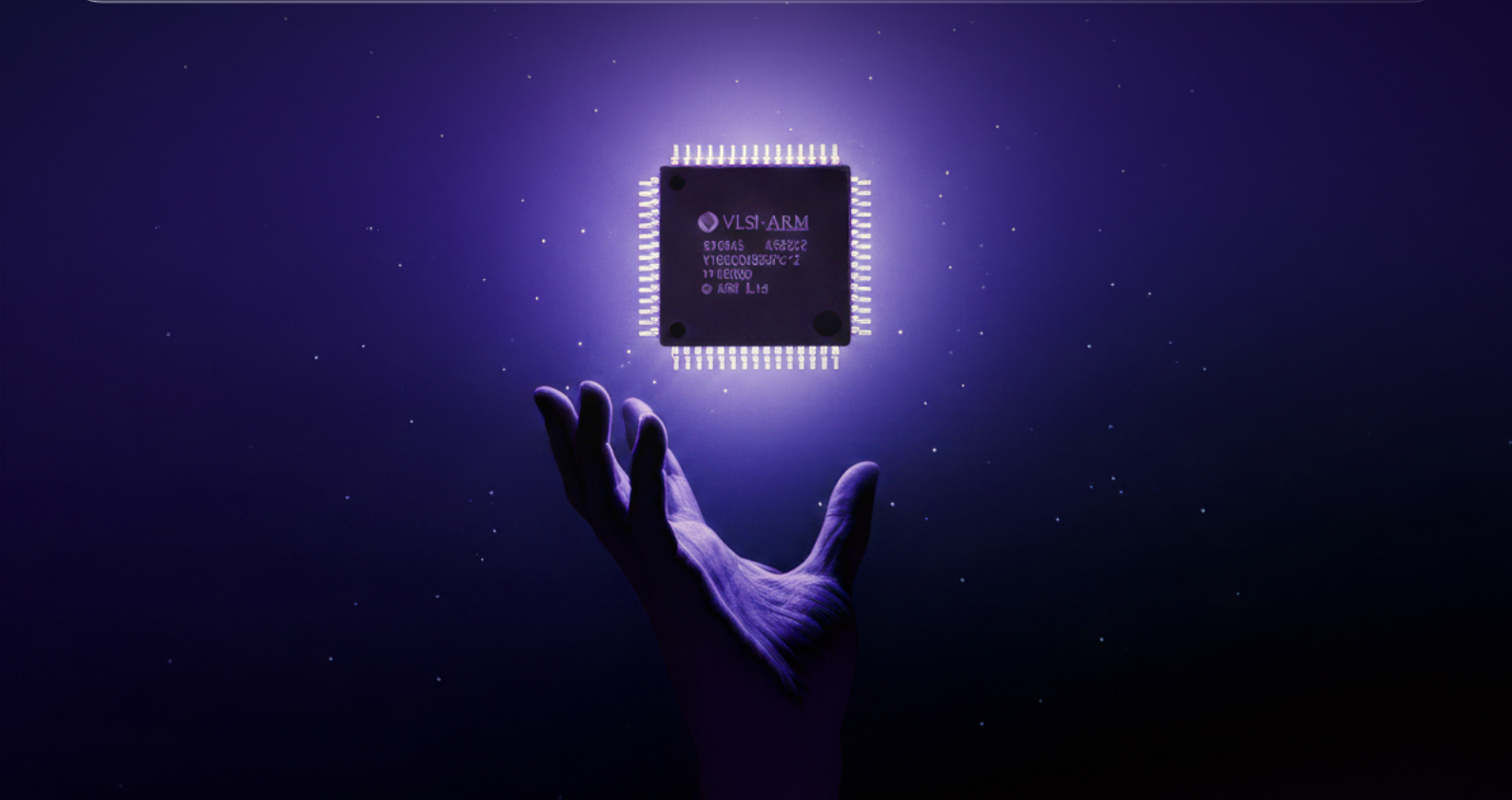
Extensive focus on **Low-Power RTL** and **UPF awareness**, including production-ready Clock Gating labs.

AI-Integrated EDA

Learn to make use of AI for Design Space Exploration (DSE) and timing closure.

Evidence-First Pedagogy

You don't just "learn", you build an **Evidence Pack** (Waveforms, logs, and QoR reports) that proves your proficiency to be recruited.



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Programme Faculty

Program Director

Prof. Mrigank Sharad

Assistant Professor, Rajendra Mishra School of Engineering Entrepreneurship, Indian Institute of Technology Kharagpur

Expertise

VLSI Design, Digital and Mixed Signal IC Design, VLSI for AI and ML, Neuromorphic Computing

Prof. Indrajit Chakrabarti

Professor, Department of Electronics & Electrical Communication Engineering, Indian Institute of Technology Kharagpur

Expertise

VLSI Architectures for Image and Video Processing, Digital and Analog VLSI Design, Signal Processing Architectures for Communication Systems

Prof. Amit Kumar Dutta

Associate Professor, G.S. Sanyal School of Telecommunication, Indian Institute of Technology Kharagpur

Expertise

Physical Layer Communication Theory, Quantum Signal Processing, THz Communication, 6G Communications, VLSI Architecture for Communication Systems

Your 8-Month Journey

MODULE 1:
Verilog & Combinational RTL Foundations

Weeks 1-2

- Digital Design Foundations
- Verilog Onboarding + First Verified Module
- Combinational Modeling Styles + Decoder Design (QoR Awareness)

MODULE 2:
Sequential RTL & FSM Controllers

Weeks 3-5

- Verilog System Design Essentials (Job-Aligned) + Code Experiments
- Sequential RTL: DFFs & Counters (ASIC Flow Awareness)
- FSM Controllers: Sequence, Vending Machine & Elevator Models
- Vivado Flow Literacy

MODULE 3:
Memory Blocks & Datapath Design

Weeks 6-10

- Memory in RTL: Register File, RAM & FIFO (FPGA + ASIC)
- Datapath vs Control Logic
- Fixed-Point Arithmetic, Truncation & Approximation Safety

MODULE 4:

Low-Power RTL & AI-Augmented Power Aware Architecture

Weeks 11-13

- Design for power, not just functionality
- Power Fundamentals I: 4 Power Types + Activity Tracing
- Low-Power Techniques: 6 Key Levers
- Power-Aware Architecture Design
- Clock Gating Cell RTL (Production-Ready) + Verification

MODULE 5:

FPGA Workflow & Cadence Synthesis Workflow / STA Literacy

Weeks 14-16

- Bridge FPGA and ASIC thinking
- FPGA vs ASIC Synthesis Differences
- Cadence Synthesis & STA: Genus + Tempus
- TCL Scripting, Optimization using AI

MODULE 6:

Capstone Kickoff

Weeks 16-18

- Capstone Kickoff: (Spec→Architecture) + (Algorithm→RTL Plan)
- Capstone Build I: Controller FSM, FIFOs & Testbench
- Capstone Build II: Constraints, QoR Optimization for PPA

MODULE 7:
Physical Design Foundations

Week 19-20

- RTL→GDSII Baseline Run
- Cadence P&R Baseline using Innovus
- AI-Assisted QoR Analysis & Iterative Improvements

MODULE 8:
Floorplanning & Power Planning Foundations

Weeks 21-22

- Placement + Congestion Mitigation (Power tie-in)
- CTS + Routing Overview + Clock Power Intuition

MODULE 9:
RTL → GDSII Deep Dive & Signoff

Weeks 23-28

- Cadence RTL → GDSII Baseline (Canonical Block)
- Tool Awareness & Mapping to Open-Source Flows
- Floorplanning & Locality (Power & Toggling Awareness)
- Placement & Congestion Mitigation
- CTS, Routing & Process / Corner Variations
- Signoff Literacy: DRC, LVS & UPF Power Intent
- Power Analysis & Multi-Knob Optimization (Voltus / Joules)

MODULE 10:

AI-Driven Low Power Co-Optimization

Weeks 29-30

- ML-Based Architecture Design Space Exploration (DSE)
- AI-Guided QoR Tuning Loop
- Predictive STA & ECO Recommendations (Bounded)
- Congestion & Floorplan Prediction

MODULE 11:

Portfolio & Interview Readiness

Week 31

- Translate skills into job-ready outcomes
- Portfolio Curation & Project Storytelling
- Interview Readiness for RTL, PD & AI-EDA Roles

MODULE 12:

Capstone Closure & Commercial Low-Power Methodology Showcase

Week 32

- Capstone Report Showcase
- Commercial Low-Power Methodology Showcase (Cadence-based) - demo + decision memo

Sample Captsone Projects

01 Hardware-Accelerated Audio Signal Processing with Neural Network Classifier

Project Overview	Design and implement a hardware-optimized audio feature extraction pipeline (FFT/MFCC-based) integrated with a lightweight neural network classifier.
Focus Areas	Fixed-point DSP implementation, pipelined FFT architecture, feature extraction hardware blocks, quantized neural network inference, RTL simulation and validation.
Industry Relevance	Voice-enabled systems, automotive speech interfaces, wake-word detection, low-power edge AI hardware.

02 Tiny YOLO-Based Object Detection Accelerator for Edge AI

Project Overview	Develop a streamlined CNN accelerator capable of executing Tiny YOLO inference targeted for FPGA.
Focus Areas	Convolution engine architecture, MAC array design, memory bandwidth optimization, INT8 quantization, pipeline optimization, RTL-to-FPGA implementation flow awareness.
Industry Relevance	Smart surveillance systems, edge vision devices, drones, robotics.

03 Accelerator for Optical Flow Estimation and Object Detection for Automated Vehicles

Project Overview	Understand hardware acceleration pipeline supporting optical flow computation and object detection to enable real-time perception in automated vehicle systems.
Focus Areas	Parallel processing architecture, motion vector computation blocks, CNN inference acceleration, memory hierarchy optimization, latency-aware RTL design.
Industry Relevance	Advanced Driver Assistance Systems (ADAS), autonomous vehicles, real-time perception hardware, automotive AI chips.

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Your Credential

Receive an **IIT Kharagpur Certificate** and Executive Alumni Status on successful completion

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Tools & Technologies

Digital VLSI Design & ASIC Physical Design

This program delivers hands-on, industry-aligned training in Digital Front-End Design and ASIC Physical Design, covering the complete RTL-to-GDSII flow used by modern semiconductor companies.

Digital Design (Front-End)

- Verilog for RTL design and verification
- RTL simulation, debugging, and waveform analysis
- Logic synthesis with standard cell libraries
- Constraint development using SDC
- Static Timing Analysis (STA) for setup/hold and clock analysis
- TCL scripting for flow automation and design optimization

Physical Design (Back-End)

- Floor planning and power planning
- Standard cell placement and timing-driven optimization
- Clock Tree Synthesis (CTS) and skew management
- Global and detailed routing
- Physical verification: DRC, LVS awareness
- Post-layout STA and sign-off awareness

Industry Tools & Environment VIVADO and Cadence EDA Fusion:

- **Vivado IDE** along with **100 Hours** of Hands-on Access to **Cadence** Industry Tools Chain.
- Learners work directly on **Cadence Genus, Innovus, Xcelium, and Tempus**, mirroring real-world ASIC design and physical implementation workflows.

SOP for Cadence Tool Usage

Each candidate receives **100 hours (50 slots)** of dedicated, high-performance access to the **industry-standard Cadence suite,** managed through a structured slot-booking system to ensure fair and optimal usage across all learners. Slots are treated as committed assets, **unutilized or partially used slots are deducted from the candidate's personal credit slot bucket**, reflecting the professional standards of a VLSI industry environment. Candidates are required to book their preferred slots one month in advance based on direction by the faculty, with the flexibility to revise preferences at the start of each new month.

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Career Outcomes

VLSI Design Engineer	RTL Design Engineer	Chip Architect	Low-Power Design Engineer
₹8 - 22 LPA	₹8 - 18 LPA	₹12 - 27 LPA	₹12 - 30 LPA
FPGA Design Engineer	Physical Design Engineer	SoC Design Engineer	ASIC Design Engineer
₹8 - 20 LPA	₹8 - 25 LPA	₹15 - 35 LPA	₹10 - 28 LPA

*Indicative salary ranges based on Indian semiconductor hiring trends

Who Should Apply?

- **4th Year B.E/ B. Tech students**
  willing to kick start their career in VLSI
- **Fresh Graduates**
  Interested in VLSI Design careers
- **Early/Mid Career**
  0-3 Years Experience in VLSI/other job areas

Refer to the Eligibility page for the exact eligibility criteria.

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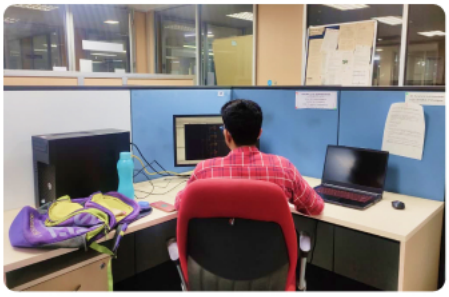
Campus Immersion

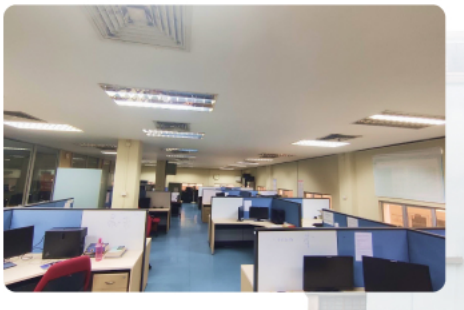
Your Graduation at the Gateway of Excellence

Celebrate your 32-week journey where it all began. The program concludes with a **Two day Exclusive In-Person visit to the IIT Kharagpur campus**.

- **Network with Giants**: Meet your cohort and the IIT faculty face-to-face.
- **Experience the Legacy**: Get the feeling of being an IITian, meet on campus students and expand your vision.
- **Silicon Networking**: Direct interaction with people doing Cutting edge Research using IIT Research facility.








Learning Outcomes

01

DIGITAL DESIGN & RTL MASTERY

Design synthesizable RTL using Verilog, applying digital logic, FSM design, and industry-standard coding practices for real chip design workflows.

02

FUNCTIONAL VERIFICATION SKILLS

Build verification environments with testbenches, assertions, and waveform analysis to validate functionality and debug complex digital designs.

03

VLSI DESIGN FLOW UNDERSTANDING

Understand the complete VLSI lifecycle, from RTL and synthesis to physical design, timing analysis, AI/Assisted fine tuning and sign-off awareness.

04

PHYSICAL DESIGN & PPA AWARENESS

Implement designs using Industry standard tools & analyze power, performance, and area (PPA) trade-offs across floorplanning, placement, & routing stages.

05

LOW-POWER & SYSTEM-LEVEL THINKING

Apply low-power VLSI techniques and understand how chip-level design decisions impact performance, reliability, and embedded system behavior.

06

INDUSTRY-READY PORTFOLIO OUTCOMES

Graduate with hands-on VLSI projects, a complete end-to-end capstone, and design artefacts aligned with semiconductor interview expectations.

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Futurense Bridge Course

Before the PG Certificate in VLSI Design begins, every learner undergoes a **Structured Bridge Course Designed to Build Strong Technical Fundamentals in Electronics and VLSI Concepts**. This ensures all learners, regardless of background, enter the program prepared, confident, and **Day-1 ready**.

Bridge Course Focus

Build essential electronics and VLSI foundations so learners can seamlessly transition into advanced VLSI design coursework with clarity and confidence.

What You'll Learn

- Semiconductor Material & Analog Basics
- GenAI, Agentic AI and Prompt Engineering
- System Thinking for AI
- Digital Electronics & HDL Foundations

Learning Structure

- Weekly 4 hours of live online training
- 30+ hours of self-paced learning material
- Engaging interactive sessions led by industry experts.
- Assessment at the end of the course to ensure readiness

Outcome

Begin the IIT Kharagpur VLSI program with strong fundamentals, improved technical clarity, and the academic readiness required to **Excel in both Coursework and Hands-on Design from Day 1**.

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Career Assistance

Profile, Narrative & Resume Building 01

Craft a recruiter-ready identity with optimized resumes, LinkedIn profiles, and a strong career narrative.

Career-Specific Training 02

Develop job-ready skills with role-focused training, capability tests, AI tools workshops, and continuous upskilling to match real hiring expectations.

Futurense Job Board - Exclusive Opportunities 03

Access curated, pre-vetted roles before they hit public portals, with priority visibility for Futurense learners.

Interview Playbooks & Cheat Sheets 04

Get insider interview guidance with structured playbooks: FAQs, sample answers, frameworks, recruiter insights, and round-wise preparation.

Mock Interviews with Experts 05

Experience real interview simulations with personalized feedback from mentors, industry leaders, and FLC members.

Mentor Referrals & Networking 06

Unlock referral advantages, insider recommendations, alumni-driven opportunities, and FLC mentorship that accelerates your career entry.

Salary Negotiation Support 07

Get guidance on positioning, benchmarking, negotiation strategy, and communication to secure the compensation you deserve.

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What Futurense Learners Say

Thrishakthi V

Programming Executive

★★★★★

The programs are designed in a way that helps me strengthen my technical skills, gain practical exposure, and stay updated with the latest developments in my field. The supportive environment, knowledgeable faculty, and flexible learning structure make it easier to balance work and studies while still growing academically. Overall, Futurense has truly helped me upgrade my skills and prepare more confidently for future opportunities.

Krishna Vardhan

Firmware Engineer

★★★★★

I truly got the opportunity to learn and explore my full potential here. Today, I'm giving my best while working on a research paper under my professor's guidance. I'm grateful to Futurense for providing all the support that made this journey possible.

Thousif Shaik

Senior Design Engineer

★★★★★

The VLSI program offers excellent industry-oriented learning with strong faculty support and real-time project exposure. The curriculum connects advanced VLSI and semiconductor concepts directly to practical work. It's perfect for working professionals aiming to upgrade skills while continuing their careers and helped same for me.

Vedant Mehrotra

Director

★★★★★

The VLSI course provided a comprehensive understanding of semiconductor devices and integrated circuit design, blending rigorous theoretical concepts with practical exposure to industry-relevant tools like Sentaurus and Vivado. It strengthened my analytical and design skills, and equipped me with the technical depth and confidence essential for pursuing advanced work in VLSI and semiconductor technology.

Dharma Khimavath Rahul Naik

Verification engineer

★★★★★

I'm grateful for the incredible journey I had in the VLSI Design program through Futurense. The engaging courses and hands-on training really pushed me to grow. I wholeheartedly recommend this program to anyone passionate about VLSI design!

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Eligibility

Educational Qualification

- Eligibility: B.Tech/B.E (4th Year Students or Completed)/ M.Tech/M.E in Electronics, ECE, EE, VLSI, Electrical, Instrumentation, CS, IT, M.E, Minor in Electronics or CS with B.Tech/B.E in any field and allied branches.
- M.Sc (Electronics / Physics / Semiconductor Technology).

Minimum Academic Requirement

- 50% aggregate (or equivalent CGPA).

Work Experience

- Currently in 4th Year of BTech / UG program/ PG student/ Graduated Fresher / Working Professional.
- **Special Consideration:** Candidates from other engineering disciplines with demonstrable exposure to Embedded systems, Digital Electronics, HDL, or Semiconductor fundamentals may be considered on a case-by-case basis.

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The Path (Admissions)

STEP 01

Apply Online

Submit your professional profile and academic background

STEP 02

Shortlist

Profiles are screened for technical readiness

STEP 03

Entrance

Online entrance exam

STEP 04

Enroll

Block your seat and begin the **Onboarding** pre-work

FEE DETAILS

Program Fee	Application Fee	Campus Immersion
₹1.25 LAKHS + 18% GST	₹5,000 (INCLUDED IN THE PROGRAM FEE)	₹10,000 (APPROXIMATELY)

- No-Cost EMI Available: Learners opting for an education loan can avail of No-Cost EMI for loan tenures up to 6 months, subject to applicable terms and approval.
- Scholarship for Upfront Payment: Learners choosing to make the full program fee payment upfront are eligible for a scholarship of up to INR 6,000 on the total program fee (inclusive of GST) of INR 1,47,500.

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About Futurense

Futurense is **India's Fastest-growing AI-skilling Company,** dedicated to accelerating India's role in global AI development.

With projections from the **EY's "India@100"** report, indicating that **24.3% of the Incremental Global Workforce** over the next decade will be Indians by 2030, we are committed to positioning India at the forefront of AI evolution.

Our mission is to scientifically map AI talent demand and create scalable, industry-aligned upskilling models that equip Indian professionals with cutting-edge capabilities. By integrating real-world applications with academic excellence, we are building tomorrow's leaders across every possible funnel, shaping the talent that will define tomorrow.

Impact & Ecosystem

3M+ LEARNER COMMUNITY

70+ UNIVERSITY COLLABORATIONS

10+ IIT/IIM PARTNERSHIPS

540+ TRUSTED HIRING PARTNERS

100+ MENTORS & EXPERTS

25K+ CAREERS TRANSFORMED

400+ FUTURENSE TEAM STRENGTH

65+ ENTERPRISE CLIENTS ACROSS FORTUNE 500 AND GCCS

Our Four Verticals

Futurense.uni

Online degree and certificate programs in partnership with IITs and IIMs.

Futurense Global

First-of-its-kind study abroad and credit transfer programs with leading global universities.

Futurense SCHOOL OF AI

Co-branded AI-focused undergraduate programs for select universities, managed end-to-end.

Futurense.enterprise

Staffing and corporate reskilling solutions for Fortune 500 companies and global capability centers (GCCs).